WHAT IS CLAIMED IS:

1. A differential register, comprising:

an input conveying an input signal;

a first pass device coupled to the input and enabling conveyance of a first signal in response to the input signal;

a second pass device coupled to the input and enabling conveyance of a second signal in response to the input signal, wherein the second signal is the compliment of the first signal; and

a first storage node coupled to the first pass device and coupled to the second pass device, the first storage node storing the first signal in response to the first pass device enabling conveyance of the first signal and the first storage node storing the second signal in response to the second pass device enabling conveyance of the second signal.

2. A differential register as set forth in claim 1, wherein the first pass device and the second pass device are controlled by the same clock.

3. A differential register as set forth in claim 1, wherein a second storage node is coupled between the input and the first pass device and the second storage node is coupled between the input and the second pass device, the second storage node storing a value in response to the input signal and the first pass device enabling conveyance of the first signal in response to the value and the second pass device enabling conveyance of the second signal in response to the value.

4. A differential register as set forth in claim 3, further comprising an input pass device coupled between the input and the storage node, the input pass device enabling conveyance of the input signal, the storage node storing the value in response to the input pass device enabling conveyance of the input signal.

5. A differential register as set forth in claim 4, wherein the input pass device is controlled by a clock signal and the first pass device and the second pass device are controlled by the compliment of the clock signal.

6. A differential register as set forth in claim 3, further comprising a first inverter coupled between the storage node and the second pass device, the first inverter generating the second signal in response to the value stored in the storage node.

7. A differential register as set forth in claim 1, further comprising a second inverter coupled to the storage node, the second inverter generating an output.

8. A differential register as set forth in claim 7, further comprising a third inverter coupled to the storage node, the third inverter generating a compliment of the output.

9. A circuit, comprising:

an input conveying an input signal;

a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal;

a first storage node coupled to the first pass gate and storing the first signal;

a second pass gate coupled to the first storage node and enabling a second signal in response to the first signal stored in the storage node and in response to a slave clock signal, wherein the slave clock generates is a compliment to the clock signal;

a first inverter coupled to the first storage node and generating a first inverted signal in response to the first signal stored in the storage node;

a third pass gate coupled to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and

a second storage node coupled to the second pass gate and coupled to the third pass gate, the second storage node storing the second signal and the third signal.

10. A circuit as set forth in claim 9, further comprising a second inverter coupled to the second storage node, the second inverter generating an output signal and a third inverter coupled to the second storage node, the third inverter generating a compliment of the output signal.

11. A circuit as set forth in claim 10, wherein the first storage node further comprises a fourth inverter and a fifth inverter configured as back-to-back inverters.

12. A circuit as set forth in claim 11, wherein the second storage node further comprises a sixth inverter and a seventh inverter configured as back-to-back inverters, wherein the sixth inverter is weak relative to the fourth inverter.

13. A circuit as set forth in claim 10, wherein the second storage node further comprises a fourth inverter and a fifth inverter configured as back-to-back inverters.

14. A circuit as set forth in claim 13, wherein the fourth inverter is a weak inverter relative to the first inverter.

15. A method of operating a differential register, the differential register comprising an output node, a complimentary output node and a storage node coupled between the output node and the complimentary output node, the method comprising the steps of:

storing a first value in the storage node;

storing the compliment of the first value in the storage node; and

on power-up, conveying the first value stored in the storage node out of the output node and conveying the compliment of the first value stored in the storage node out of the compliment of the output node.

16. A method of operating a differential register as set forth in claim 15 further comprising the step of conveying the first value stored in the storage node out of the output node and conveying the compliment of the first value stored in the storage node out of the compliment of the output node in response to settling effects in the storage node.

17. A differential register, comprising:

an input means for conveying an input signal;

a first pass means for conveying a first signal in response to the input signal;

a second pass means for conveying a second signal in response to the input signal, wherein the second signal is the compliment of the first signal;

a storage means for storing the first signal and storing the second signal;

a first output means for generating a first output in response to the first signal stored in the storage means; and

a second output means for generating a compliment of the first output in response to the second signal stored in the storage node.